

24V, 15A Monolithic Step Down Regulator with Differential Output Sensing

DESCRIPTION

FEATURES

- Wide V_{IN} Range: 4.5V to 24V;
 V_{OUT} Range: 0.6V to 5.5V at up to 15A
- 0.67% Output Voltage Accuracy
- Controlled On-Time Valley Current Mode Architecture, Excellent Current Sharing Capability
- Frequency Programmable from 200kHz to 1MHz and Synchronizable to External Clock
- R_{SENSE} or Inductor DCR Current Sensing With Accurate Current Limit
- Fast Transient Response
- Differential Output Voltage Sensing Allowing 500mV Common Mode Remote Ground
- $t_{ON(MIN)} = 65ns$; $t_{OFF(MIN)} = 105ns$
- Overvoltage Protection and Current Limit Foldback
- Power Good Output Voltage Monitor
- Voltage Tracking Start-Up
- External V_{CC} Input for Bypassing Internal LDO
- Micropower Shutdown: $I_Q = 15\mu A$
- 7mm $\times$ 9mm 56-pin QFN Package

APPLICATIONS

- Distributed Power System
- Point-of-Load Converters
- Servers

The LTC[®]3613 is a monolithic synchronous step-down switching regulator capable of regulating outputs from 0.6V to 5.5V with up to 15A output current. The controlled on-time constant frequency valley current mode architecture allows for both fast transient response and constant frequency switching in steady-state operation, independent of V_{IN} , V_{OUT} and load. This also provides excellent current sharing capability.

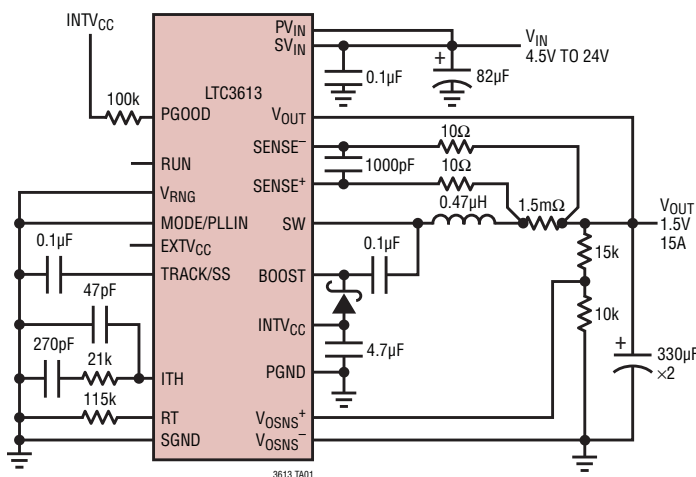
Differential output voltage sensing along with a precision internal reference combine to offer $\pm 0.67\%$ output regulation, even if the output ground reference deviates from local ground by 500mV. The switching frequency can be programmed from 200kHz to 1MHz with an external resistor. The switching frequency is also phase synchronizable to an external clock in applications where switching noise/EMI reduction is crucial.

Very low t_{ON} and t_{OFF} times allow for near 0% and near 100% duty cycles, respectively. Voltage tracking soft start-up is provided for tracking and sequencing applications. Safety features include output overvoltage protection, programmable current limit with foldback, and power good monitoring.

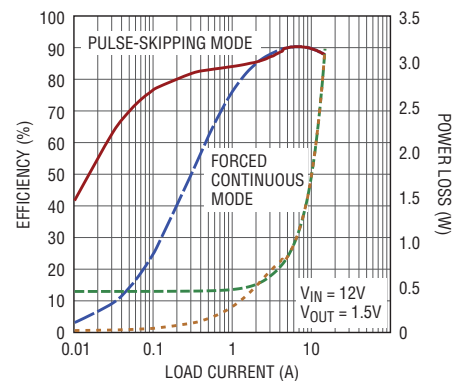
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TYPICAL APPLICATION

High Efficiency High Power Step-Down Converter



Efficiency and Power Loss vs Load Current

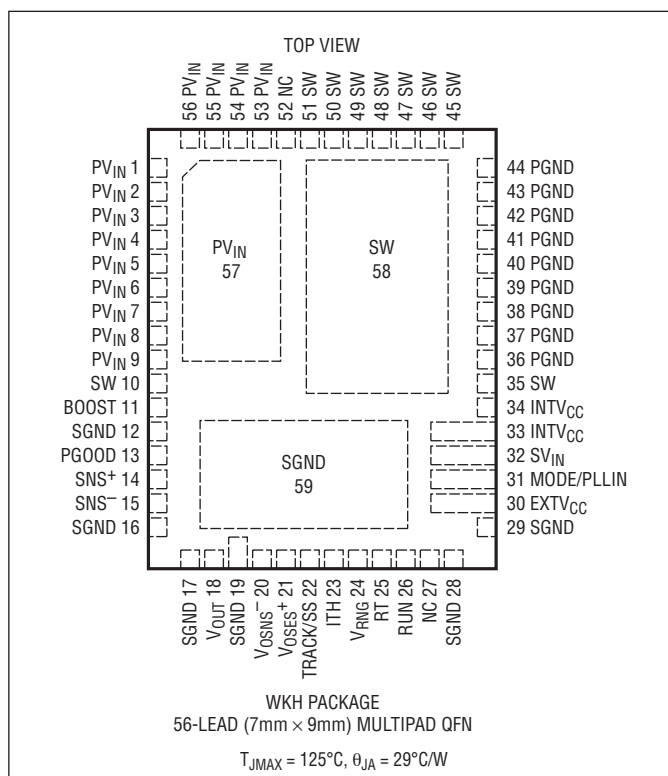


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (PV_{IN} , SV_{IN})	–0.3V to 24V
Boost Voltage	–0.3V to 30V
SW Voltage	–0.3V to 24V
$INTV_{CC}$, $EXTV_{CC}$, (BOOST-SW), MODE /PLLIN, V_{RNG} , PGOOD, RUN Voltages	–0.3V to 6V
V_{OSNS}^{+} , V_{OSNS}^{-} Voltages	–0.6V to ($INTV_{CC} + 0.3V$)
V_{OUT} , SENSE ⁺ , SENSE [–] Voltages	–0.6V to 6V
RT, ITH Voltages	–0.3V to ($INTV_{CC} + 0.3V$)
TRACK/SS Voltages	–0.3V to 5V
Operating Junction Temperature Range (Notes 2, 4)	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3613EWKH#PBF	LTC3613EWKH#TRPBF	LTC3613WKH	56-Lead (7mm × 9mm) Plastic QFN	–40°C to 125°C
LTC3613IWKH#PBF	LTC3613IWKH#TRPBF	LTC3613WKH	56-Lead (7mm × 9mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $SV_{IN} = 15\text{V}$, $V_{FB} = V_{OSNS^+} - V_{OSNS^-}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{IN}	Input Voltage Operating Range		●	4.5		24	V
V_{OUT}	Output Voltage Operating Range		●	0.6		5.5	V
I_Q	Input DC Supply Current Normal Shutdown Supply Current	MODE/PLLIN = INTV _{CC} RUN = 0V			2 15	4 25	mA μA
V_{REG}	Regulated Differential Feedback Voltage ($V_{OSNS^+} - V_{OSNS^-}$)	$I_{TH} = 1.2\text{V}$ (Note 3) $T_A = 25^\circ\text{C}$	●	0.5985	0.6	0.6015	V
		$T_A = 0^\circ\text{C to } 85^\circ\text{C}$	●	0.596	0.6	0.604	V
		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$	●	0.594	0.6	0.606	V
	Regulated Differential Feedback Voltage Over Line, Load and Common Mode ($V_{OSNS^+} - V_{OSNS^-}$)	$V_{IN} = 4.5\text{V to } 24\text{V}$, $I_{TH} = 0.5\text{V to } 1.9\text{V}$, $V_{OSNS^-} = \pm 500\text{mV}$ (Note 3)					
		$T_A = 0^\circ\text{C to } 85^\circ\text{C}$ $T_A = -40^\circ\text{C to } 125^\circ\text{C}$	● ●	0.594 0.591	0.6 0.6	0.606 0.609	V V
$t_{ON(MIN)}$	Minimum On-Time				65		ns
$t_{OFF(MIN)}$	Minimum Off-Time				105		ns
$g_m(EA)$	Error Amplifier Transconductance	$I_{TH} = 1.2\text{V}$ (Note 3)	●	1.4	1.7	2	mS
$V_{SENSE(MAX)}$	Valley Current Sense Threshold, $V_{SENSE^+} - V_{SENSE^-}$, Peak Current = Valley + Ripple	$V_{RNG} = 2\text{V}$, $V_{FB} = 0.57\text{V}$	●	80	100	120	mV
		$V_{RNG} = 0\text{V}$, $V_{FB} = 0.57\text{V}$	●	22	30	38	mV
		$V_{RNG} = \text{INTV}_{CC}$, $V_{FB} = 0.57\text{V}$	●	39	50	61	mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold, $V_{SENSE^+} - V_{SENSE^-}$, Force Continuous Operation	$V_{RNG} = 2\text{V}$, $V_{FB} = 0.63\text{V}$			-50		mV
		$V_{RNG} = 0\text{V}$, $V_{FB} = 0.63\text{V}$			-15		mV
		$V_{RNG} = \text{INTV}_{CC}$, $V_{FB} = 0.63\text{V}$			-25		mV
$V_{SENSE(CM)}$	SENSE ⁺ , SENSE ⁻ Voltage Range (Common Mode)		●	-0.5		5.5	V
I_{SENSE}	SENSE ⁺ , SENSE ⁻ Input Bias Current	$V_{SENSE(CM)} = 0.6\text{V}$ $V_{SENSE(CM)} = 5\text{V}$			±5 1	±50 4	nA μA
$V_{RUN(TH)}$	RUN Pin On Threshold	V_{RUN} Rising	●	1.1	1.2	1.3	V
$V_{RUN(HYS)}$	RUN Pin Hysteresis				80		mV
I_{SS}	Soft-Start Charging Current	$V_{TRACKSS} = 0\text{V}$			1.0		μA
UVLO	INTV _{CC} Undervoltage Lockout INTV _{CC} Undervoltage Lockout Release	Falling	●	3.4	3.65	4.0	V
		Rising	●		4.2	4.5	V
I_{VOSNS^+}	V_{OSNS^+} Input Bias Current	$V_{FB} = 0.6\text{V}$			±5	±25	nA
I_{VOSNS^-}	V_{OSNS^-} Input Bias Current	$V_{FB} = 0.6\text{V}$			-15	-50	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $S_{VIN} = 15\text{V}$, $V_{FB} = V_{OSNS}^+ - V_{OSNS}^-$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator and Clock Synchronization						
f_{OSC}	Free Running Switching Frequency	$R_T = 205\text{k}$ $R_T = 80.6\text{k}$ $R_T = 38.8\text{k}$	175 450 900	200 500 1000	225 550 1100	kHz kHz kHz
CLK_{IH}	Clock Input High Level Into Mode/PLLIN		2			V
CLK_{IL}	Clock Input Low Level Into Mode/PLLIN				0.5	V
Internal V_{CC} Regulator and External V_{CC}						
$INTV_{CC}$	Internal V_{CC} Voltage	$6\text{V} < V_{IN} < 24\text{V}$	5.1	5.3	5.55	V
$INTV_{CC}(\%)$	Internal V_{CC} Load Regulation	$I_{CC} = 0\text{mA}$ to 50mA		-1	-2	%
$EXTV_{CC}(\text{TH})$	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Rising	4.4	4.6	4.75	V
$EXTV_{CC}(\text{HYS})$	$EXTV_{CC}$ Switchover Hysteresis			200		mV
$\Delta INTV_{CC}$	$EXTV_{CC}$ Voltage Drop	$V_{EXTV_{CC}} = 5\text{V}$, $I_{CC} = 50\text{mA}$		200		mV
PGOOD Output						
PGD_{OV}	PGOOD Upper Threshold	V_{FB} Rising (With Respect to Regulated Feedback Voltage V_{REG})	5	7.5	10	%
PGD_{UV}	PGOOD Lower Threshold	V_{FB} Falling (With Respect to Regulated Feedback Voltage V_{REG})	-10	-7.5	-5	%
PGD_{HYS}	PGOOD Hysteresis	V_{FB} Returning		2		%
$V_{PGD}(\text{LO})$	PGOOD Low Voltage	$I_{PGOOD} = 5\text{mA}$		0.15	0.4	V
$t_{PGD}(\text{FALL})$	Delay from OV/UV Fault to PGOOD Falling	(Note 5)		20		μs
$t_{PGD}(\text{RISE})$	Delay from OV/UV Recovery to PGOOD Rising	(Note 5)		10		μs
$R_{DS}(\text{ON})$						
$R_{DS}(\text{ON})$	Top Switch On-Resistance Bottom Switch On-Resistance			7.5 5.5		mohm mohm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature, T_A , and power dissipation, P_D , as follows:

$$T_J = T_A + (P_D \cdot 29^\circ\text{C/W}) \quad (\theta_{JA} \text{ is simulated per JESD51-7 high effective thermal conductivity test board})$$

$$\theta_{JC} = 1^\circ\text{C/W} \quad (\theta_{JC} \text{ is simulated when heat sink is applied at the bottom of the package.})$$

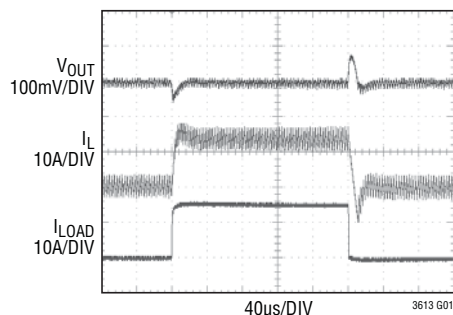
Note 3: The LTC3613 is tested in a feedback loop that adjusts $V_{FB} = V_{OSNS}^+ - V_{OSNS}^-$ to achieve a specified error amplifier output voltage (ITH).

Note 4: The LTC3613 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3613E is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3613I is guaranteed over the full -40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 5: Delay times are measured using 50% levels.

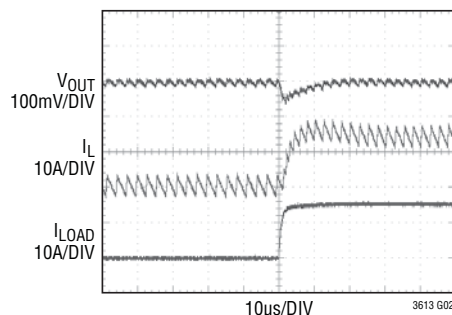
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

**Transient Response:
Forced Continuous Mode**



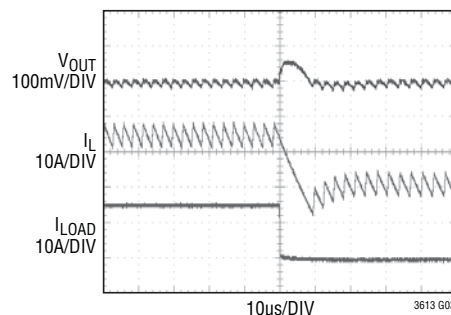
LOAD TRANSIENT = 0A TO 15A
 $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

**Load Step:
Forced Continuous Mode**



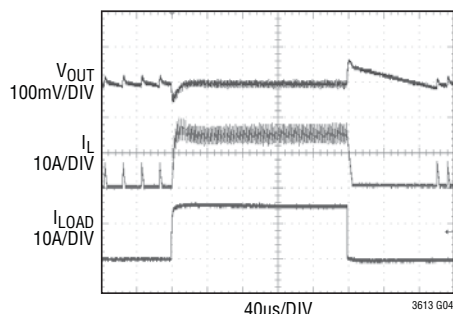
LOAD STEP = 0A TO 15A
 $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

**Load Release:
Forced Continuous Mode**



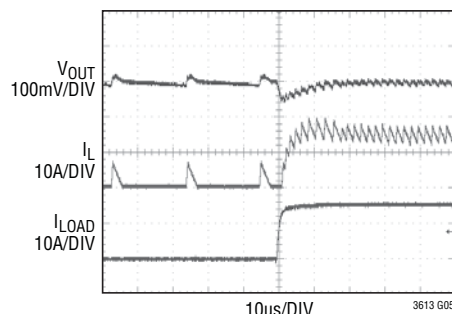
LOAD RELEASE = 15A TO 0A
 $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

**Transient Response:
Pulse-Skipping Mode**



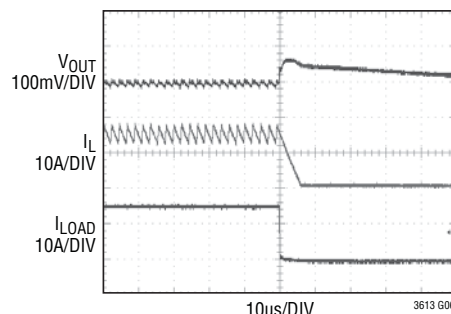
LOAD TRANSIENT = 500mA TO 15A
 $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

Load Step: Pulse-Skipping Mode



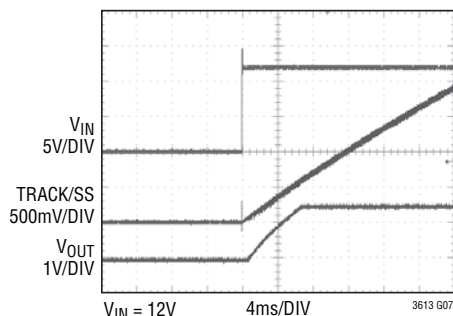
LOAD STEP = 500mA TO 15A
 $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

**Load Release:
Pulse-Skipping Mode**



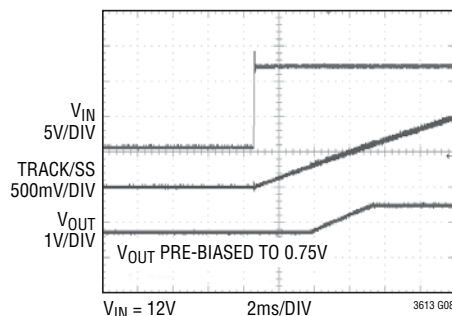
LOAD RELEASE = 15A TO 500mA
 $V_{IN} = 12\text{V}$, $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

Normal Soft Start-Up



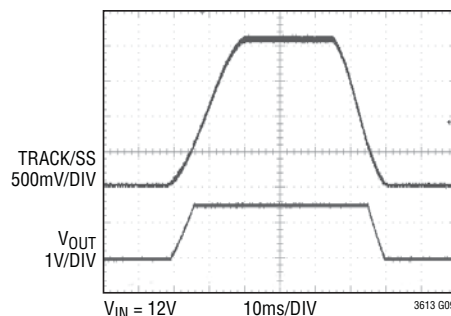
$V_{IN} = 12\text{V}$
 $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

**Soft Start-Up into
a Pre-Biased Output**



$V_{IN} = 12\text{V}$
 $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

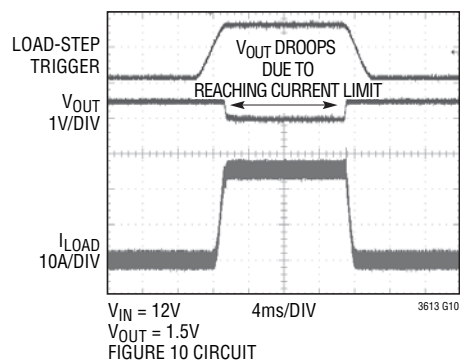
Output Tracking



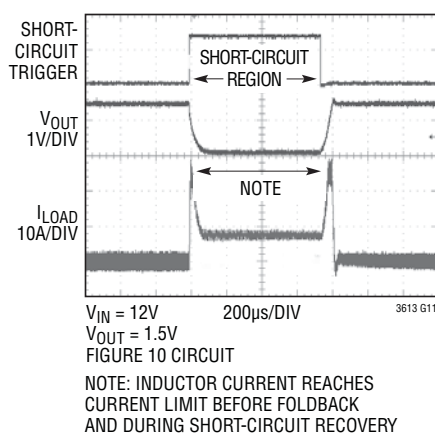
$V_{IN} = 12\text{V}$
 $V_{OUT} = 1.5\text{V}$
FIGURE 10 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

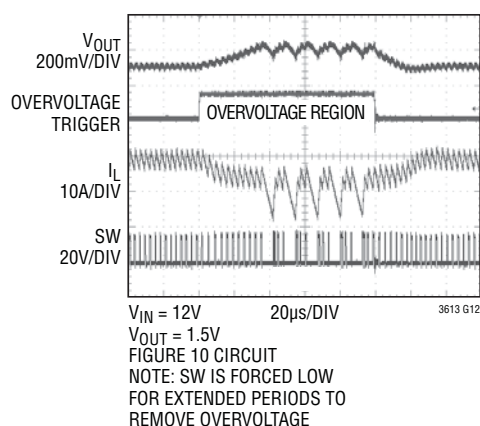
Overcurrent Protection



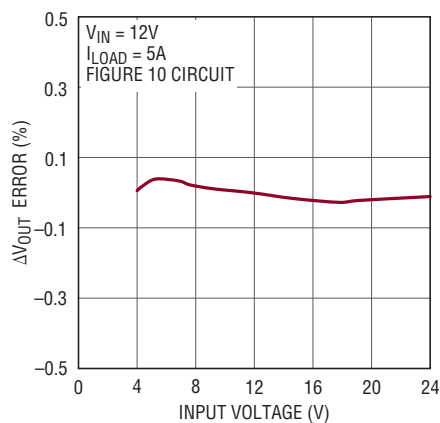
Short-Circuit Protection



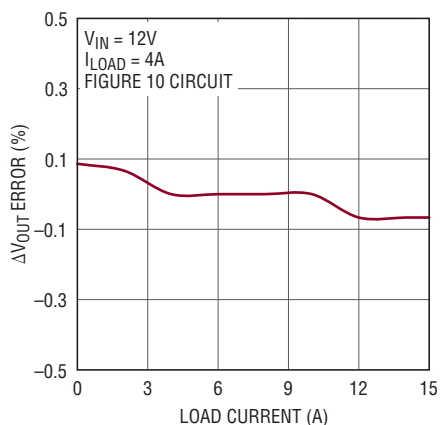
Overvoltage Protection



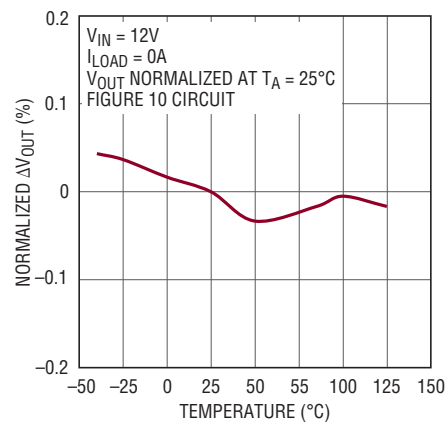
Output Regulation vs Input Voltage



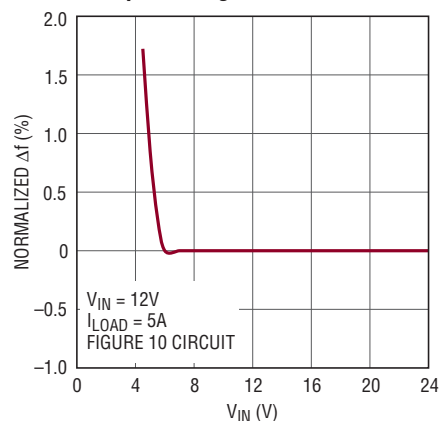
Output Regulation vs Load Current



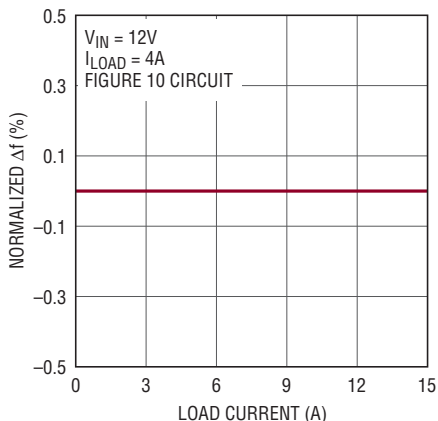
Output Regulation vs Temperature



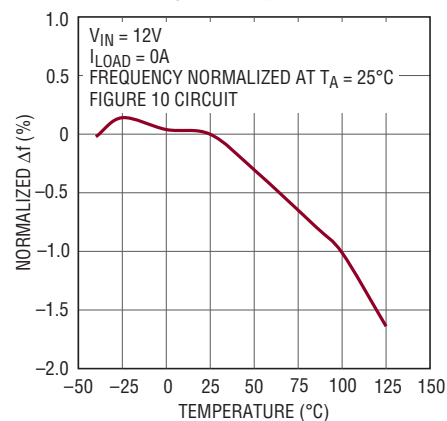
Switching Frequency vs Input Voltage



Switching Frequency vs Load Current

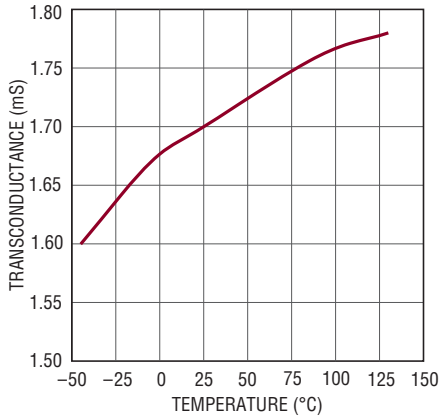


Non-Synchronized Switching Frequency vs Temperature

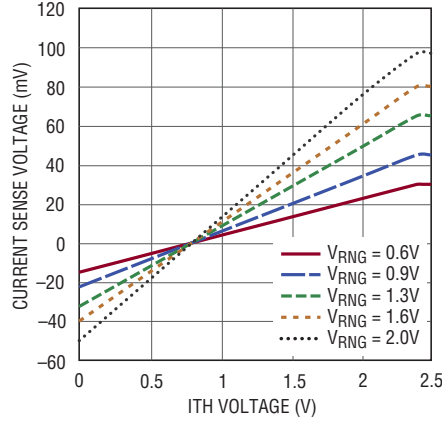


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

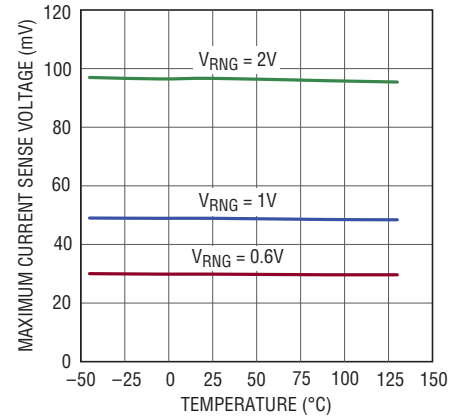
Error Amplifier Transconductance vs Temperature



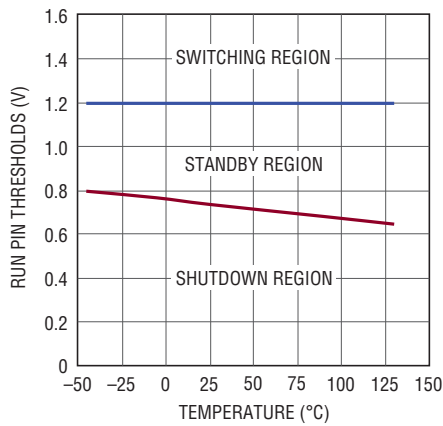
Current Sense Voltage vs ITH Voltage



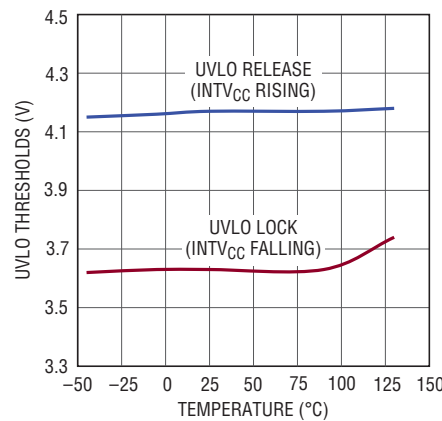
Maximum Current Sense Voltage vs Temperature



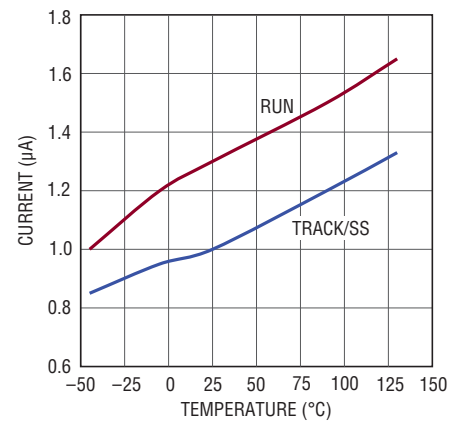
RUN Thresholds vs Temperature



Input Undervoltage Lockout Thresholds vs Temperature



RUN and TRACK/SS Pull-Up Currents vs Temperature



PIN FUNCTIONS

PV_{IN} (Pins 1-9, 53-56, 57 Exposed Pad): Power Supply Inputs. These pins connect to the drain of the internal power MOSFETS. The PV_{IN} exposed pad must be soldered to the circuit board for electrical contact and rated thermal performance. The supply voltage can range from 4.5V to 24V. The voltage on this pin is also used to adjust the TG on-time in order to maintain constant frequency operation.

SW (Pins 10, 35, 45-51, 58 Exposed Pad): Switch Node Connection. The (–) terminal of the bootstrap capacitor, C_B, connects to this node. This pin swings from a diode voltage below ground up to V_{IN}. The SW exposed pad must be soldered to the circuit board for electrical contact and rated thermal performance.

BOOST (Pin 11): Boosted Driver Supply Connection. The (+) terminal of the bootstrap capacitor, C_B, as well as the cathode of the Schottky diode, D_B, connects to this node. This node swings from INTV_{CC} – V_{SCHOTTKY} to V_{IN} + INTV_{CC} – V_{SCHOTTKY}.

SGND (Pins 12, 16, 17, 19, 28, 29, 59 Exposed Pad): Signal Ground Connection. The SGND exposed pad must be soldered to the circuit board for electrical contact and rated thermal performance. All small-signal components should be connected to the signal ground. Connect signal ground to power ground only at one point using a single PCB trace.

PGOOD (Pin 13): Power Good Indicator Output. This open-drain logic output is pulled to ground when the output voltage is outside of a $\pm 7.5\%$ window around the regulation point.

SENSE⁺ (Pin 14): Differential Current Sensing (+) Input. For R_{SENSE} current sensing, Kelvin (4-wire) connect SENSE⁺ and SENSE[–] pins across the sense resistor. For DCR sensing, Kelvin connect SENSE⁺ and SENSE[–] pins across the sense filter capacitor.

SENSE[–] (Pin 15): Differential Current Sensing (–) Input. For R_{SENSE} current sensing, Kelvin (4-wire) connect the SENSE⁺ and SENSE[–] pins across the sense resistor. For DCR sensing, Kelvin connect the SENSE⁺ and SENSE[–] pins across the sense filter capacitor.

V_{OUT} (Pin 18): Output voltage sense for adjusting the on-time for constant frequency operation. Tying this pin to the local output (instead of the remote output) is recommended for most applications. This pin can be programmed as needed for achieving the steady-state on-time required for constant frequency operation.

V_{OSNS}[–] (Pin 20): Differential Output Sensing (–) Input. Connect this pin to the negative terminal of the output capacitor. There is a bias current of 35 μ A (typical) flowing out of this pin.

V_{OSNS}⁺ (Pin 21): Differential Output Sensing (+) Input. Connect this pin to the feedback resistor divider between the positive and negative output capacitor terminals. In normal operation the LTC3613 will regulate the differential output voltage which is divided down to 0.6V by the feedback resistor divider.

TRACK/SS (Pin 22): External Tracking and Soft-Start Input. The LTC3613 regulates the differential feedback voltage (V_{OSNS}⁺ – V_{OSNS}[–]) to the smaller of 0.6V or the voltage on the TRACK/SS pin. An internal 1.0 μ A pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. Alternatively, another voltage supply connected through a resistor divider to this pin allows the output to track the other supply during start-up.

ITH (Pin 23): Current Control Voltage and Switching Regulator Compensation Point. The current sense threshold increases with this control voltage which ranges from 0V to 2.4V.

V_{RNG} (Pin 24): Current Sense Voltage Range Input. The maximum allowed sense voltage between SENSE⁺ and SENSE[–] is equal to $0.05 \cdot V_{RNG}$. If V_{RNG} is tied to SGND, the device operates with a maximum sense voltage of 30mV. If V_{RNG} is tied to INTV_{CC}, the device operates with a maximum sense voltage of 50mV.

RT (Pin 25): Switching Frequency Programming Pin. Connect an external resistor from RT to signal ground to program the switching frequency between 200kHz and 1MHz. An external clock applied to MODE/PLLIN must be within $\pm 30\%$ of this free-running frequency to ensure frequency lock.

PIN FUNCTIONS

RUN (Pin 26): Digital Run Control Input. RUN self biases high with an internal 1.3 μ A pull-up. Forcing RUN below 1.2V disables switching. Taking RUN below 0.75V shuts down all bias and places the LTC3613 into micropower shutdown mode of approximately 15 μ A.

EXTV_{CC} (Pin 30): External V_{CC} Input. When EXTV_{CC} exceeds 4.6V, an internal switch connects this pin to INTV_{CC} and shuts down the internal regulator so that the controller and gate drive power is drawn from EXTV_{CC}. EXTV_{CC} should not exceed V_{IN}.

MODE/PLLIN (Pin 31): External Clock Synchronization Input and/or Forced Continuous Mode Input. When an external clock is applied to this pin, the rising switching cycle will be synchronized with the rising edge of the external clock. Additionally, this pin determines operation under light load conditions. When either a clock input is

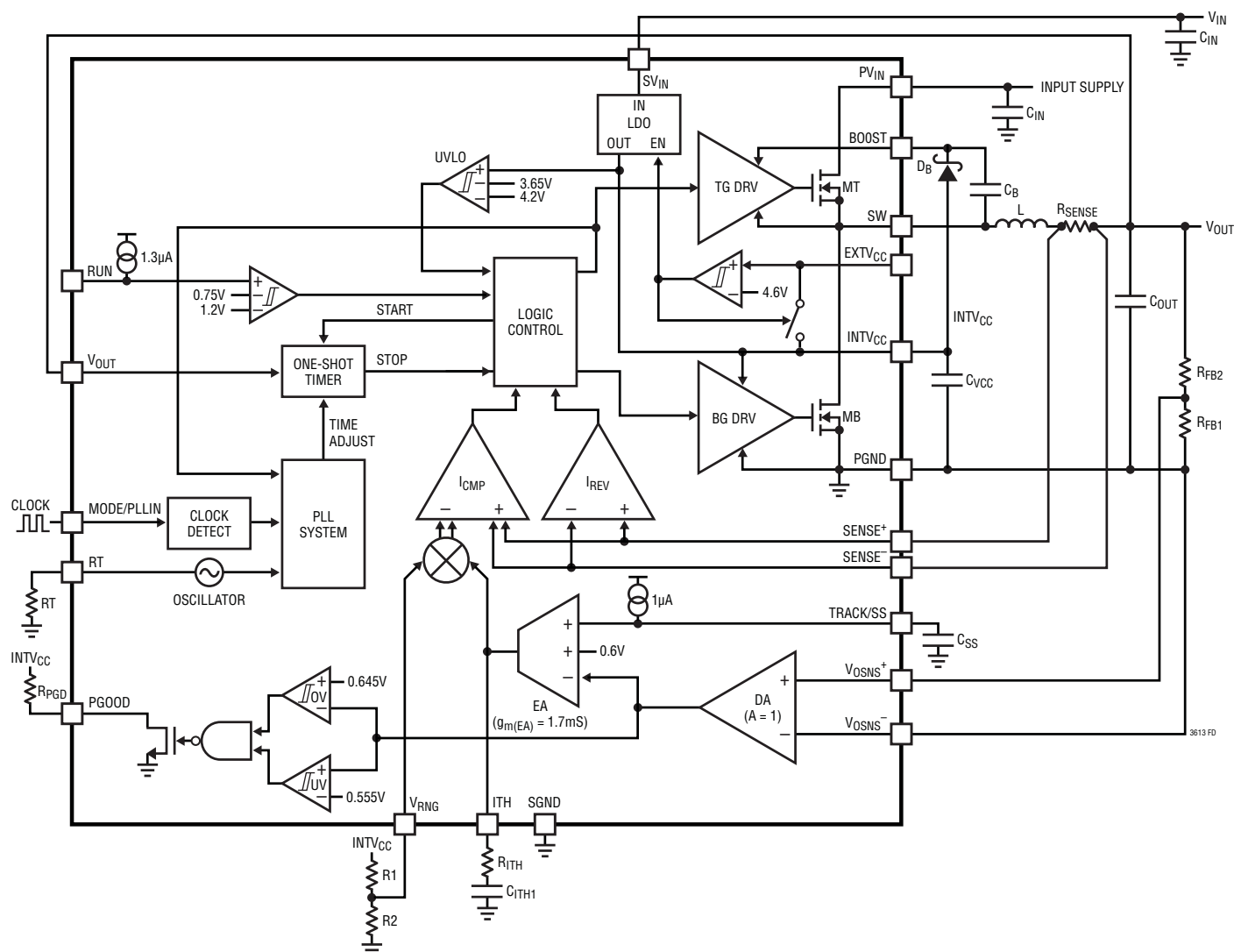
detected or MODE/PLLIN is tied to INTV_{CC}, forced continuous mode operation is selected. Tying this pin to SGND allows discontinuous pulse-skipping mode operation at light loads.

SV_{IN} (Pin 32): Signal Input Supply. This pin powers the internal control circuitry.

INTV_{CC} (Pins 33, 34): Internal 5.3V Regulator Output. The driver and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7 μ F ceramic capacitor (C_{VCC}). The anode of the Schottky diode, D_B, connects to this pin.

PGND (Pins 36-44): Power Ground Connection. Connect this pin as close as practical to the (–) terminal of C_{VCC} and the (–) terminal of C_{IN}.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3613 uses valley current mode control to regulate the output voltage in a monolithic, all N-channel MOSFET DC/DC step-down converter. Current control is achieved by sensing the inductor current across SENSE⁺ and SENSE⁻, either by using an explicit resistor connected in series with the inductor or by implicitly sensing the inductor's resistive (DCR) voltage drop through an RC filter connected across the inductor.

In normal steady-state operation, the top MOSFET is turned on for a fixed time interval proportional to the delay in the one-shot timer. The PLL system adjusts the delay in the one-shot timer until the top MOSFET turn-on is synchronized either to the internal oscillator or the external clock input if provided. As the top MOSFET turns off, the bottom MOSFET turns on with a small time delay (dead time) to avoid shoot-through current. The next switching cycle is initiated when the current comparator, I_{CMP}, senses that inductor current has reached the valley threshold point

OPERATION (Refer to Functional Diagram)

and turns the bottom MOSFET off immediately and the top MOSFET on. Again in order to avoid shoot-through current there is a small dead time delay before the top MOSFET turns on.

The voltage on the ITH pin sets the I_{CMP} valley threshold point. The error amplifier, EA, adjusts this ITH voltage by comparing the differential feedback signal, $V_{OSNS}^+ - V_{OSNS}^-$, to a 0.6V internal reference voltage. Consequently, the LTC3613 regulates the output voltage by forcing the differential feedback voltage to be equal to the 0.6V internal reference. The difference amplifier, DA, converts the differential feedback signal to a single-ended input for the EA. If the load current increases, it causes a drop in the differential feedback voltage relative to the reference. The EA forces ITH voltage to rise until the average inductor current again matches the load current.

Differential Output Sensing

The output voltage is resistively divided externally to create a feedback voltage for the controller. The internal difference amplifier, DA, senses this feedback voltage along with the output's remote ground reference to create a differential feedback voltage. This scheme overcomes any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage. The LTC3613 allows for remote output ground deviations as much as $\pm 500\text{mV}$ with respect to local ground.

INTV_{CC}/EXTV_{CC} Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the INTV_{CC} pin. Power on the INTV_{CC} pin is derived in two ways: if the EXTV_{CC} pin is below 4.6V, then an internal 5.3V low dropout linear regulator, LDO, supplies INTV_{CC} power from PV_{IN}; if the EXTV_{CC} pin is tied to an external source larger than 4.6V, then the LDO is shut down and an internal switch shorts the EXTV_{CC} pin to the INTV_{CC} pin, thereby powering the INTV_{CC} pin with the external source and helping to increase overall efficiency and decrease internal self heating through power dissipated in the LDO. This external power source could be the output of the step-down switching regulator itself if the output is programmed to higher than 4.6V.

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B , which normally recharges during each off cycle through an external Schottky diode when the top MOSFET turns off. If the V_{IN} voltage is low and INTV_{CC} drops below 3.65V, undervoltage lockout circuitry disables the external MOSFET driver and prevents the power switches from turning on.

Shutdown and Start-Up

The LTC3613 can be shut down using the RUN pin. Pulling this pin below 1.2V prevents switching, and less than 0.75V disables most of the internal bias circuitry, including the INTV_{CC} regulator. When RUN is less than 0.75V, the shutdown I_Q is about 15 μA . Pulling the RUN pin between 0.75V and 1.2V enables the controller into a standby mode where all internal circuitry is powered-up except for the MOSFET driver. The standby I_Q is about 2mA. Releasing the RUN pin from ground allows an internal 1.3 μA current to pull the pin above 1.2V and fully enable the controller including the MOSFET driver. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin. When pulled up by a resistor to an external voltage, the RUN pin will sink about 35 μA of current before reaching 6V. If the external voltage is above 6V (e.g., V_{IN}), select a large enough resistor value so that the voltage on RUN will not exceed 6V.

The start-up of the output voltage, V_{OUT} , is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.6V internal reference, the LTC3613 regulates the differential feedback voltage to the TRACK/SS voltage instead of the 0.6V reference. This allows the TRACK/SS pin to be used for programming a ramp-up time for V_{OUT} by connecting an external capacitor from the TRACK/SS pin to SGND. An internal 1 μA pull-up current charges this capacitor, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises from 0V to 0.6V (and beyond), the LTC3613 forces the output voltage, V_{OUT} , to ramp up smoothly to its final value. Alternatively, the TRACK/SS pin can be used to track the start-up of V_{OUT} to another external supply as in a master slave configuration. Typically, this requires connecting a resistor divider from the master supply to the TRACK/SS pin (see Soft-Start and Tracking).

OPERATION

When the RUN pin is pulled low to disable the controller or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3.65V, the TRACK/SS pin is pulled low internally.

Light Load Current Operation

When the DC load current is less than 1/2 of the peak-to-peak inductor current ripple, the inductor current can drop to zero or become negative. If the MODE/PLLIN pin is connected to SGND, the LTC3613 will transition into discontinuous mode operation (also called pulse-skipping mode), where a current reversal comparator, I_{REV} , detects and prevents negative inductor current by shutting off the bottom MOSFET, MB. In this mode, both switches remain off with the output capacitor supplying the load current. As the output capacitor discharges and the output voltage droops lower, the EA will eventually move the ITH voltage above the zero current level to initiate another switching cycle.

If the MODE/PLLIN pin is tied to $INTV_{CC}$ or an external clock is applied to MODE/PLLIN, the LTC3613 will be forced to operate in continuous mode (forced continuous mode) and not transition into discontinuous mode. In this case the current reversal comparator, I_{REV} , is disabled, allowing the inductor current to become negative and thus maintain constant frequency operation.

Frequency Selection and External Clock Synchronization

The steady-state switching frequency of the LTC3613 is set by an internal oscillator. The frequency of this internal oscillator can be programmed from 200kHz to 1MHz by connecting a resistor from the RT pin to SGND. The RT pin is forced to 1.2V internally. A phase-locked loop (PLL) system synchronizes the turn-on of the switching cycle to this internal oscillator when no external clock is provided.

For applications with stringent frequency or interference requirements, an external clock source connected to the MODE/PLLIN pin can be used to synchronize the

switching cycle turn-on to the rising edge of the clock. The LTC3613 operates in forced continuous mode when it is synchronized to the external clock. The external clock frequency has to be within $\pm 30\%$ of the internal oscillator frequency for successful synchronization and the clock input levels should be greater than 2V for HI and less than 0.5V for LO. The MODE/PLLIN pin has an internal 600k Ω pull-down resistor.

Power Good and Fault Protection

The power good pin, PGOOD, is connected internally to an open-drain N-channel MOSFET. An external pull-up resistor to a voltage supply of up to 6V (or $INTV_{CC}$) completes the power good detection scheme. Overvoltage and undervoltage comparators OV and UV turn on the MOSFET and pull the PGOOD pin low when the differential feedback voltage is outside a $\pm 7.5\%$ window of the 0.6V reference voltage. The PGOOD pin is also pulled low when the LTC3613 is in the soft-start or tracking phase, when in undervoltage lockout, or when the RUN pin is low (shut down).

When the differential feedback voltage is within the $\pm 7.5\%$ requirement, the open-drain NMOS is turned off and the pin is pulled up by an external resistor. There is an internal delay of 10 μ s before the PGOOD pin will indicate power good once the differential feedback voltage is within the $\pm 7.5\%$ window. When the feedback voltage goes out of the $\pm 7.5\%$ window, there is an internal 20 μ s delay before PGOOD is pulled low. In an overvoltage condition, MT is turned off and MB is turned on immediately without any delay and held on until the overvoltage condition clears.

Foldback current limiting is provided if the output is shorted to ground. As the differential feedback voltage drops, the current threshold voltage on the ITH pin is pulled down and clamped to 1.2V. This reduces the inductor valley current level to one-fourth of its maximum value as the differential feedback approaches 0V. Foldback current limiting is disabled at start-up.

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The Typical Application on the first page of this data sheet is a basic LTC3613 application circuit. The LTC3613 can be configured to sense the inductor current either through a series sense resistor, R_{SENSE} , or through an RC filter across the inductor (DCR). The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Once the required output voltage and operating frequency have been determined, external component selection is driven by load requirements, and begins with the selection of inductor and current sensing components. Next, the proper current sense threshold is programmed using the V_{RNG} pin. Finally, input and output capacitors are selected.

Output Voltage Programming and Differential Output Sensing

The LTC3613 integrates differential output sensing with output voltage programming, allowing for simple and seamless design. As shown in Figure 1, the output voltage is programmed by an external resistor divider from the regulated output point to its ground reference. The resistive divider is tapped by the V_{OSNS}^+ pin, and the ground reference is sensed by V_{OSNS}^- . An optional feed-forward capacitor, C_{FF} , can be used to improve the transient performance of the regulator system as discussed under OPTI-LOOP® Compensation. The resulting output voltage is given according to the following equation:

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}} \right)$$

More precisely, the V_{OUT} value programmed in the previous equation is with respect to the output's ground reference, and thus is a differential quantity. For example, if V_{OUT} is programmed to 5V and the output ground reference is at -0.5V, then the output will be 4.5V with respect to signal ground. The minimum differential output voltage is limited to the internal reference, 0.6V, and the maximum differential output voltage is 5.5V.

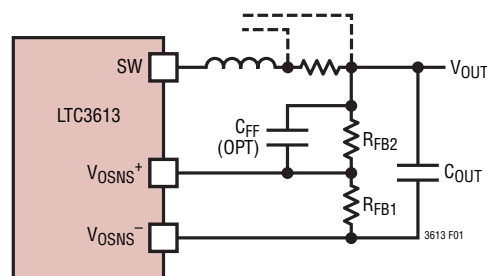


Figure 1. Setting Output Voltage

The V_{OSNS}^+ pin is high impedance with no input bias current. The V_{OSNS}^- pin has about 35 μ A of current flowing out of the pin.

Differential output sensing allows for more accurate output regulation in high power distributed systems having large line losses. Figure 2 illustrates the potential variations in the power and ground lines due to parasitic elements. These variations are exacerbated in multi-application systems with shared ground planes. Without differential output sensing, these variations directly reflect as an error in the regulated output voltage. The LTC3613's differential output sensing can correct for up to ± 500 mV of variation in the output's power and ground lines.

The LTC3613's differential output sensing scheme is distinct from conventional schemes where the regulated output and its ground reference are directly sensed with a difference amplifier whose output is then divided down with an external resistive divider and fed into the error amplifier input. This conventional scheme is limited by the common mode input range of the difference amplifier and typically limits differential sensing to the lower range of output voltages.

The LTC3613 allows for seamless differential output sensing by sensing the resistively divided feedback voltage differentially. This allows for differential sensing in the full output range from 0.6V to 5.5V. The difference amplifier of the LTC3613 has a -3dB bandwidth of 8MHz, high enough to not affect main loop compensation and transient behavior.

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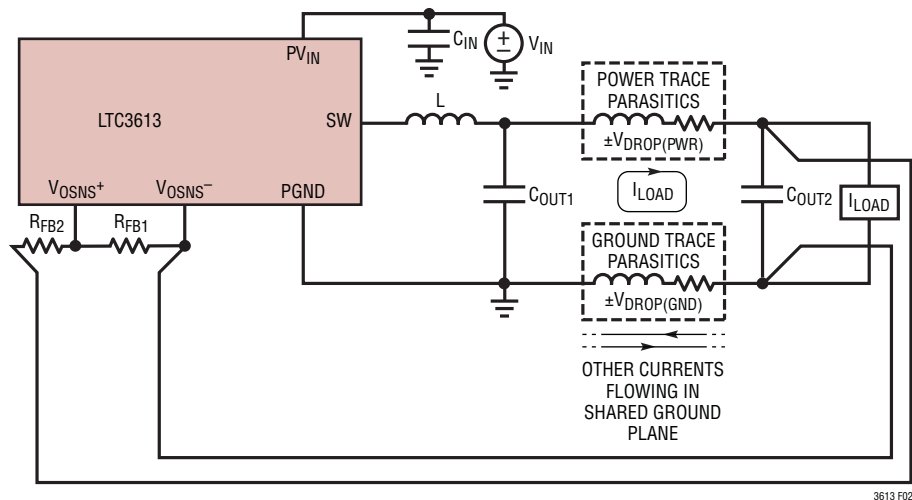


Figure 2. Differential Output Sensing Used to Correct Line Loss Variations in a High Power Distributed System with a Shared Ground Plane

To avoid noise coupling into V_{OSNS}^+ , the resistor divider should be placed near the V_{OSNS}^+ and V_{OSNS}^- pins and physically close to the LTC3613. The remote output and ground traces should be routed together as a differential pair to the remote output. These traces should be terminated as close as physically possible to the remote output point that is to be accurately regulated through remote differential sensing.

Switching Frequency Programming

The choice of operating frequency is a trade-off between efficiency and component size. Lowering the operating frequency improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. Conversely, raising the operating frequency degrades efficiency but reduces component size.

The switching frequency of the LTC3613 can be programmed from 200kHz to 1MHz by connecting a resistor from the RT pin to signal ground. The value of this resistor is given by the following empirical formula:

$$R_T [k\Omega] = \frac{41550}{f [kHz]} - 2.2$$

Not counting resistor tolerances, the switching frequency could still have a $\pm 10\%$ deviation from the ideal programmed value. The internal PLL has a synchronization range of $\pm 30\%$ around this programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this $\pm 30\%$ range of the RT programmed frequency. It is advisable that the RT programmed frequency be equal to the external clock for maximum synchronization margin. Refer to Phase and Frequency Synchronization for further details.

Inductor Selection

The operating frequency and inductor selection are inter-related in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses and top MOSFET transition losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

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The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L , decreases with higher inductance or frequency and increases with higher V_{IN} :

$$\Delta I_L = \frac{V_{OUT}}{f \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, higher ESR losses in the output capacitor, and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4 \cdot I_{OUT(MAX)}$ where $I_{OUT(MAX)}$ is the maximum output current for the application. The maximum ΔI_L occurs at the maximum input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \cdot \Delta I_{L(MAX)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot tolerate the core loss of low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy or Kool M μ cores. Ferrite core material saturates *hard*, meaning that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft, Toko, Vishay, Pulse and Würth.

Current Sense Pins and Current Limit Programming

Inductor current is sensed through the SENSE⁺ and SENSE⁻ pins and fed into the internal current comparators. The common mode input voltage range of the cur-

rent comparators is -0.5V to 5.5V. Both SENSE pins are high impedance inputs. When the common mode range is between -0.5V to 1.1V, there is no input bias current, and when between 1.4V and 5.5V, there is less than 1 μ A of current flowing into the pins. Between 1.1V and 1.4V, the input bias current will be zero if the common mode voltage is ramped up from 1.1V and less than 1 μ A if the common mode voltage is ramped down from 1.4V. The high impedance inputs to the current comparator allow accurate DCR sensing. However, care must be taken not to float these pins during normal operation.

The maximum allowed sense voltage $V_{SENSE(MAX)}$ between SENSE⁺ and SENSE⁻ is set by the voltage applied to the V_{RNG} pin and is given by:

$$V_{SENSE(MAX)} = 0.05 \cdot V_{RNG}$$

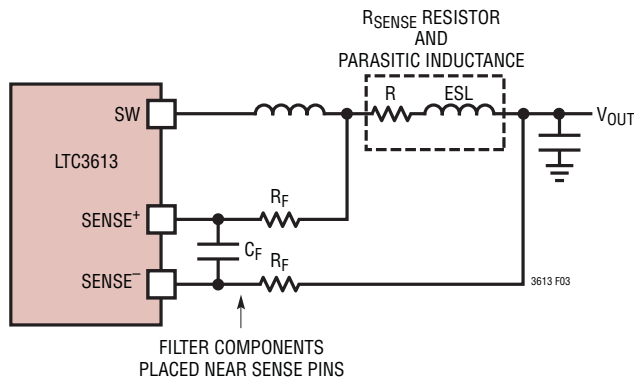
The current mode control loop does not allow the inductor current valleys to exceed $0.05 \cdot V_{RNG}$. The maximum output current is given by:

$$I_{OUT(MAX)} = \frac{V_{SENSE(MAX)}}{R_{SENSE}} + \frac{1}{2} \Delta I_L$$

The $V_{SENSE(MAX)}$ is shown in the figure "Maximum Current Sense Voltage vs Temperature" in the Typical Performance Characteristics. Note that ITH is close to 2.4V when in current limit.

An external resistive divider from INTV_{CC} can be used to set the voltage on the V_{RNG} pin between 0.6V and 2V, resulting in maximum sense voltages between 30mV and 100mV. The wide voltage sense range allows for a variety of applications. The V_{RNG} pin can also be tied to either SGND or INTV_{CC} to force internal defaults. When V_{RNG} is tied to SGND, the device operates with a maximum sense voltage of 30mV. When the V_{RNG} pin is tied to INTV_{CC}, the device operates with a maximum sense voltage of 50mV. When setting current limit, ensure that the junction temperature does not exceed the rating of 125°C.

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Figure 3. R_{SENSE} Current Sensing **R_{SENSE} Inductor Current Sensing**

A typical R_{SENSE} inductor current sensing scheme is shown in Figure 3. R_{SENSE} is chosen based on the required maximum output current. Given the maximum current, $I_{\text{OUT(MAX)}}$, maximum sense voltage, $V_{\text{SENSE(MAX)}}$, set by the V_{RNG} pin, and maximum inductor ripple current, $\Delta I_L(\text{MAX})$, the value of R_{SENSE} can be chosen as:

$$R_{\text{SENSE}} = \frac{V_{\text{SENSE(MAX)}}}{I_{\text{OUT(MAX)}} - \frac{\Delta I_L(\text{MAX})}{2}}$$

Conversely, given R_{SENSE} and $I_{\text{OUT(MAX)}}$, $V_{\text{SENSE(MAX)}}$ and thus the V_{RNG} voltage could be determined from the above equation. To assure that the maximum rated output current can be supplied for different operating conditions and component variations, sufficient design margin should be built into these calculations.

Because of possible PCB noise in the current sensing loop, the current ripple of $\Delta V_{\text{SENSE}} = \Delta I_L \cdot R_{\text{SENSE}}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 10mV ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications.

For today's highest current density solutions the value of the sense resistor can be less than 1m Ω and the maximum sense voltage can be as low as 30mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions, the voltage drop across the sense resistor's parasitic inductance becomes more relevant. A small RC filter placed near the IC has been traditionally used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10 Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin (4-wire) connected to the sense resistor.

DCR Inductor Current Sensing

For applications requiring higher efficiency at high load currents, the LTC3613 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 4. The DCR of the inductor represents the small amount of DC winding resistance, which can be less than 1m Ω for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

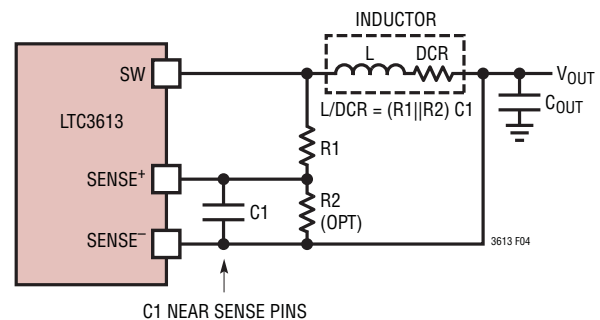


Figure 4. DCR Current Sensing

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The inductor DCR is sensed by connecting an RC filter across the inductor. This filter typically consists of one or two resistors (R1 and R2) and one capacitor (C1) as shown in Figure 4. If the external $R1 \parallel R2 \cdot C1$ time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR multiplied by $R2/(R1 + R2)$. Therefore, R2 may be used to scale the voltage across the sense terminals when the DCR is greater than the target sense resistance. With the ability to program current limit through the V_{RNG} pin, R2 may be optional. C1 is usually selected to be in the range of 0.01 μ F to 0.47 μ F. This forces $R1 \parallel R2$ to around 2k to 4k, reducing error that might have been caused by the sense pins' input bias currents.

The first step in designing DCR current sensing is to determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 25°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for inductor temperature T_L is 100°C. The DCR of the inductor can also be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' datasheets for detailed information.

From the DCR value, $V_{SENSE(MAX)}$ is calculated as:

$$V_{SENSE(MAX)} = DCR_{MAX} \text{ at } 25^\circ\text{C} \cdot \left[1 + 0.4\% (T_{L(MAX)} - 25^\circ\text{C}) \right] \cdot \left[I_{OUT(MAX)} - \Delta I_L / 2 \right]$$

If $V_{SENSE(MAX)}$ is within the maximum sense voltage of the LTC3613 as programmed by the V_{RNG} pin (30mV to 100mV), then the RC filter only needs R1. If $V_{SENSE(MAX)}$ is higher, then R2 may be used to scale down the maximum sense voltage so that it falls within range.

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}(R1) = \frac{(V_{IN(MAX)} - V_{OUT}) \cdot V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or R_{SENSE} sensing. Light load power loss can be modestly higher with a DCR network than with a sense resistor due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

To maintain a good signal-to-noise ratio for the current sense signal, use a minimum ΔV_{SENSE} of 10mV. For a DCR sensing application, the actual ripple voltage will be determined by:

$$\Delta V_{SENSE} = \frac{V_{IN} - V_{OUT}}{R1 \cdot C1} \cdot \frac{V_{OUT}}{V_{IN} \cdot f}$$

Operating Multiple Units in Parallel

The LTC3613's current mode control architecture makes it straightforward to parallel multiple units for higher output current. Figure 13 shows an example circuit of two LTC3613s placed in parallel to provide 30A at 1.2V from a 6V to 24V input. The signals at MODE/PLLIN are 180° out of phase, to reduce stress on the input and output capacitors.

Since the ITH pin voltage determines the cycle-by-cycle valley inductor current, sharing is achieved by connecting the ITH pins together. Because the ITH pin is sensitive to noise, a small 22pF to 47pF decoupling capacitor should

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be placed close to each ITH pin. If a compensation scheme is stable on a single phase application, a polyphase application with N phases should be compensated as:

$$C_{ITH1} = N \cdot C_{ITH(SINGLE)}, C_{ITH2} = N \cdot C_{ITH2(SINGLE)} \text{ and } R_{ITH} = R_{ITH(SINGLE)}/N.$$

The TRACK/SS pins should be connected together so that all LTC3613s start up with the same slew rate. The V_{OSENSE}^+ pins of paralleled LTC3613s should be connected together to prevent any false triggering of overvoltage and short circuit protection. Only one divider is necessary. The remote output and ground traces should be routed together as differential pairs and terminated at the same remote sensing location (preferably Kelvin connected across the bulk capacitors at the remote output point). The smaller value ceramic input and output capacitors, however, should be in close proximity to the ICs.

C_{IN} and C_{OUT} Selection

In continuous mode, the current into PV_{IN} is a square wave of duty cycle V_{OUT}/V_{IN} . To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \sqrt{\frac{V_{IN}}{V_{OUT}}} - 1$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings for electrolytic and conductive polymer capacitors are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required.

The selection of C_{OUT} is primarily determined by the effective series resistance, ESR, to minimize voltage ripple. The output ripple, ΔV_{OUT} , in continuous mode is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(R_{ESR} + \frac{1}{8 \cdot f \cdot C_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the peak-to-peak current ripple requirement. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. When using ceramic input capacitors, care must be taken to ensure that ringing from inrush currents and switching does not pose an overvoltage hazard to the regulator.

For high switching frequencies, reducing output ripple and better EMI filtering may require small-value capacitors that have low ESL (and correspondingly higher self resonant frequencies) to be placed in parallel with larger value capacitors that have higher ESL. This will ensure good noise and EMI filtering in the entire frequency spectrum of interest. Even though ceramic capacitors generally have good high frequency performance, small ceramic capacitors may still have to be parallel connected with large ones to optimize performance.

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Top MOSFET Driver Supply (C_B , D_B)

An external bootstrap capacitor, C_B , connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from $INTV_{CC}$ when the switch node is low. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately $PV_{IN} + INTV_{CC}$. The boost capacitor needs to store approximately 100 times the gate charge required by the top MOSFET. In most applications a 0.1 μ F to 0.47 μ F, X5R or X7R dielectric capacitor is adequate. It is recommended that the BOOST capacitor be no larger than 10% of the $INTV_{CC}$ capacitor, C_{VCC} , to ensure that the C_{VCC} can supply the upper MOSFET gate charge and BOOST capacitor under all operating conditions. Variable frequency in response to load steps offers superior transient performance but requires higher instantaneous gate drive. Gate charge demands are greatest in high frequency low duty factor applications under high dI/dt load steps and at start-up.

In order to minimize SW node ringing and EMI, connect a 5 Ω to 10 Ω resistor in series with the BOOST pin. Make the C_B and D_B connections on the other side of the resistor. This series resistor helps to slow down the SW node rise time, limiting the high dI/dt current through the top MOSFET that causes SW node ringing.

$INTV_{CC}$ Regulator and $EXTV_{CC}$ Power

The LTC3613 features a PMOS low dropout linear regulator (LDO) that supplies power to $INTV_{CC}$ from the SV_{IN} supply. $INTV_{CC}$ powers much of the LTC3613's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5.3V.

The LDO can supply a maximum current of 50mA_{RMS} and must be bypassed to ground with a minimum of 4.7 μ F ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the power MOSFET gate drivers.

When the voltage applied to $EXTV_{CC}$ pin rises above 4.6V, the $INTV_{CC}$ LDO is turned off and the $EXTV_{CC}$ is connected to $INTV_{CC}$ with an internal switch. This switch remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.4V. Using the $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from the LTC3613's switching regulator output during normal operation and from the LDO when the output is out of regulation (e.g., start-up, short circuit). If more than 50mA_{RMS} current is required through $EXTV_{CC}$, then an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that this external voltage source is less than SV_{IN} .

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the switching regulator output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5.3V LDO resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to switching regulator output $V_{OUT} > 4.6V$. This provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If a 4.6V or greater external supply is available, it may be used to power $EXTV_{CC}$ provided that the external supply is sufficient enough for MOSFET gate drive requirements.
4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage converters, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.6V.

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For applications where the main input power is less than 5.3V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the PV_{IN} input with an optional 1Ω or 2.2Ω resistor as shown in Figure 5 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ LDO and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage.

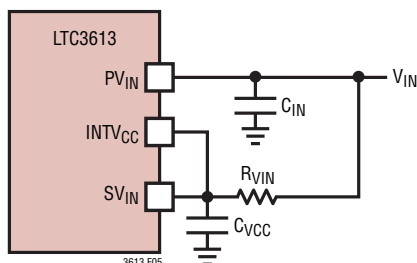


Figure 5. Setup for $V_{IN} \leq 5V$

V_{IN} Undervoltage Lockout (UVLO)

The LTC3613 has two functions that help protect the controller in case of input undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. The comparator enables UVLO and locks out the switching action until $INTV_{CC}$ rises above 4.2V. Once UVLO is released, the comparator does not retrigger UVLO until $INTV_{CC}$ falls below 3.65V. This hysteresis prevents oscillations when there are disturbances on $INTV_{CC}$.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on voltage of 1.2V, one can use a resistor divider from V_{IN} to turn on the IC when V_{IN} is high enough. The RUN pin has bias currents that depend on the RUN voltage as well as SV_{IN} voltage. These bias currents should be taken into account when designing the voltage divider and UVLO circuit to prevent faulty conditions. Generally for $RUN < 3V$ a bias current of $1.3\mu A$ flows out of the RUN pin, and for $RUN > 3V$, correspondingly increasing current flows into the pin, reaching about $35\mu A$ for $RUN = 6V$.

Soft-Start and Tracking

The LTC3613 has the ability to either soft-start by itself with a capacitor or track the output of an external supply. Soft-start or tracking features are achieved not by limiting the maximum output current of the switching regulator but by controlling the regulator's output voltage according to the ramp rate on the TRACK/SS pin.

When configured to soft-start by itself, a capacitor should be connected to the TRACK/SS pin. TRACK/SS is pulled low until the RUN pin voltage exceeds 1.2V and UVLO is released, at which point an internal current of $1\mu A$ charges the soft-start capacitor, C_{SS} , connected to TRACK/SS. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.6V on the TRACK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.6V \cdot \frac{C_{SS}}{1\mu A}$$

When the LTC3613 is configured to track another supply, a voltage divider can be used from the tracking supply to the TRACK/SS pin to scale the ramp rate appropriately. Two common implementations of tracking as shown in Figure 6 are coincident and ratiometric. For coincident tracking, make the divider ratio from the external supply the same as the divider ratio for the differential feedback voltage. Ratiometric tracking could be achieved by using a different ratio than the differential feedback (Figure 7). Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider values to be small enough to make this offset error negligible.

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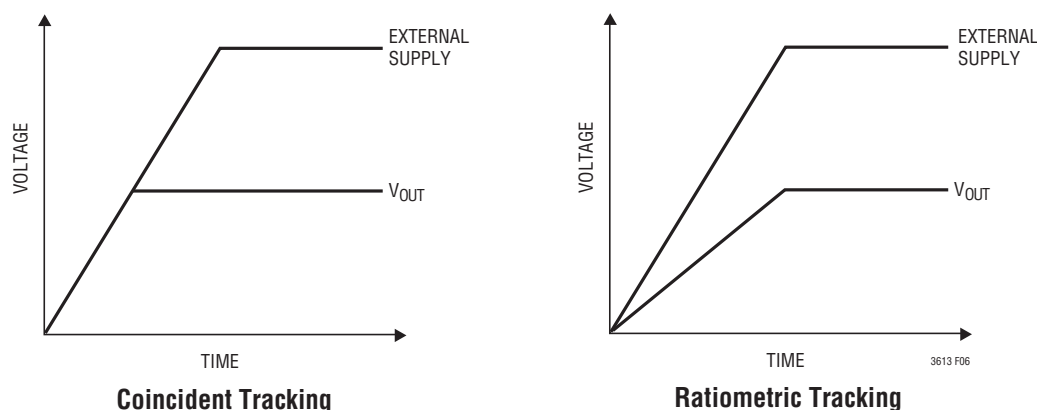


Figure 6. Two Different Modes of Output Tracking

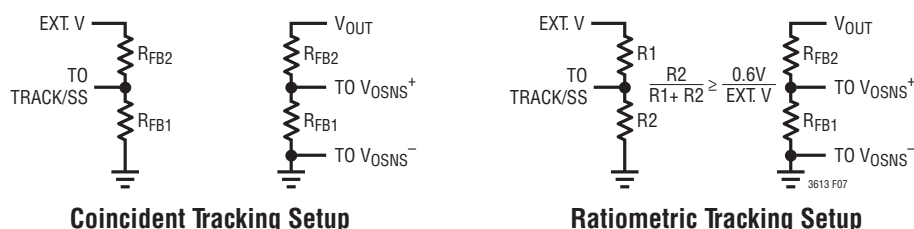


Figure 7. Setup for Coincident and Ratiometric Tracking

Phase and Frequency Synchronization

For applications that require better control of EMI and switching noise or have special synchronization needs, the LTC3613 can phase and frequency synchronize the turn-on of the switching cycle to an external clock signal applied to the MODE/PLLIN pin. The applied clock signal needs to be within $\pm 30\%$ of the RT pin programmed free-running frequency to assure proper frequency and phase lock. The clock signal levels should generally comply to $V_{IH} > 2V$ and $V_{IL} < 0.5V$. The MODE/PLLIN pin has an internal 600k pull-down resistor to ensure pulse-skipping mode if the pin is left floating.

The LTC3613 uses the voltages on SV_{IN} and V_{OUT} pins as well as the RT programmed frequency to determine the steady-state on-time as follows:

$$t_{ON} \approx \frac{V_{OUT}}{V_{IN} \cdot f}$$

An internal PLL system adjusts this on-time dynamically in order to maintain phase and frequency lock with the external clock. The LTC3613 will maintain phase and frequency lock under steady-state conditions for V_{IN} , V_{OUT} and load current.

As shown in the previous equation, the on-time is a function of the switching regulator's output. This output is measured by the V_{OUT} pin and is used to calculate the required on-time. Therefore, simply connecting V_{OUT} to the regulator's local output point is preferable for most applications. However, there could be applications where the internally calculated on-time differs significantly from the real on-time required by the application. For example, if there are differences between the local output point and the remotely regulated output point due to line losses, then the internally calculated on-time will be inaccurate. Lower efficiencies in the switching regulator can also cause the real on-time to be significantly different from the internally

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calculated on-time (see Efficiency Considerations). For these circumstances, the voltage on the V_{OUT} pin can be programmed with a resistive divider from $INTV_{CC}$ or from the regulator's output itself. Note that there is a 500k nominal resistance looking into the V_{OUT} pin.

The PLL adjusted on-time achieved after phase locking is the steady-state on-time required by the switching regulator, and if the V_{OUT} programmed on-time is substantially equal to this steady-state on-time, then the PLL system does not have to use its $\pm 30\%$ frequency lock range for systematic corrections. Instead the lock range can be used to correct for component variations or other operating point conditions. If needed, the V_{OUT} pin can be programmed to achieve the steady-state on-time as required by the application and therefore maintain constant frequency operation.

If the application requires very low on-times approaching minimum on-time, the PLL system may not be able to maintain a $\pm 30\%$ synchronization range. In fact, there is a possibility of losing phase/frequency lock at minimum on-time, and definitely losing phase/frequency lock for applications requiring less than minimum on-time. This is discussed further under Minimum On-Time, Minimum Off-Time and Dropout Operation.

During dynamic transient conditions either in the line or load (e.g., load step or release), the LTC3613 may lose phase and frequency lock in the process of achieving faster transient response. For large slew rates (e.g., 10A/ μ s), phase and frequency lock will be lost (see Figure 8) until the system returns back to a steady-state condition at which point the device will resume frequency lock and eventually achieve phase lock to the external clock. For relatively small slew rates (10A/s), phase and frequency lock can still be maintained.

For light loading conditions, the phase and frequency synchronization will be active if there is a clock input applied. If there is no clock input during light loading, then the switching frequency is based on what the MODE/PLLIN pin is tied to. When MODE/PLLIN is tied to $INTV_{CC}$, the LTC3613 will operate in forced continuous mode at the RT programmed free-running frequency. When MODE/PLLIN pin is tied to signal ground, the LTC3613 will operate in pulse-skipping discontinuous conduction mode for light loading and will switch to continuous conduction (at the free-running frequency) for normal and heavy loads.

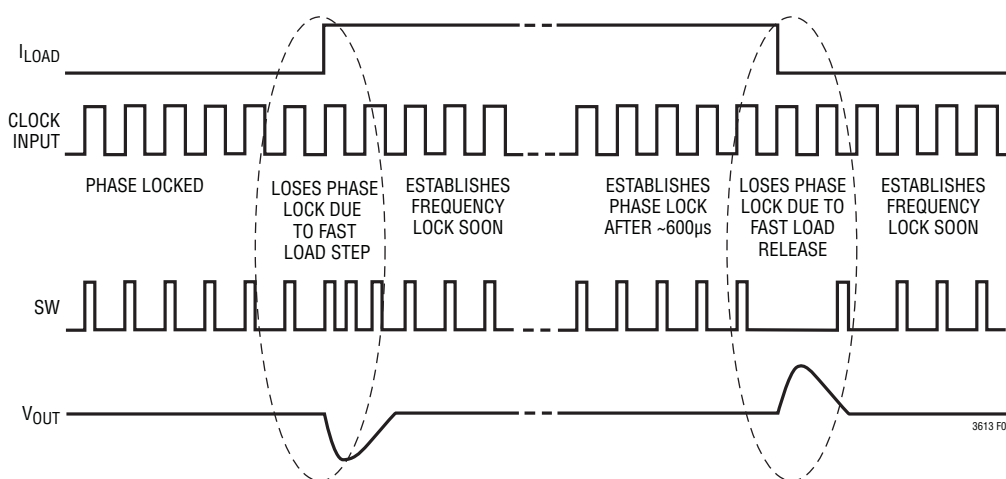


Figure 8. Phase and Frequency Locking Behavior During Transient Load Conditions

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Minimum On-Time, Minimum Off-Time and Dropout Operation

The minimum on-time is the smallest duration of time in which the LTC3613 can keep its top power MOSFET in its on state. This minimum on-time is 65ns for the LTC3613 and is achieved when the V_{OUT} pin is tied to its minimum value of 0.6V while the PV_{IN} is tied to its maximum value of 24V. For larger values of V_{OUT} or smaller values of PV_{IN} , the minimum on-time achievable will be longer than 65ns. The minimum on-time will have a dependency on the operating conditions of the switching regulator, but is intended to be smaller for high step-down ratio applications that will require low on-times.

In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$D_{MIN} = f \cdot t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the minimum on-time for the switching regulator. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

If the application requires a smaller than minimum duty cycle, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value or lose frequency synchronization if using an external clock. Depending on the application, this may not be of critical importance.

The minimum off-time is the smallest duration of time that the top power MOSFET can be turned off and then immediately turned back on. The minimum off-time that the LTC3613 can achieve is 105ns.

The minimum off-time limit imposes a maximum duty cycle of:

$$D_{MAX} = 1 - f \cdot t_{OFF(MIN)}$$

where $t_{OFF(MIN)}$ is the minimum off-time of the switching regulator. Reducing the operating frequency alleviates the maximum duty cycle constraint. If the maximum duty cycle is reached, due to a drooping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{D_{MAX}}$$

At the onset of dropout, there is a region of PV_{IN} about 500mV that generates two discrete off-times, one being the minimum off-time and the other being an off-time that is about 40ns to 60ns larger than the minimum off-time. This secondary off-time is due to the longer delay in tripping the internal current comparator. The two off-times average out to the required duty cycle to keep the output in regulation with the output ripple remaining the same. However, there is higher SW node jitter, especially apparent when synchronized to an external clock. Depending on the application, this may not be of critical importance.

Fault Conditions: Current Limiting and Overvoltage

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3613, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current mode control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \frac{V_{SENSE(MAX)}}{R_{SENSE}} + \frac{1}{2} \cdot \Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The current limit value should be greater than the inductor current required to produce maximum output power at the worst-case efficiency. Worst-case efficiency typically occurs at the highest PV_{IN} and highest ambient temperature.

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To further limit current in the event of a short circuit to ground, the LTC3613 includes foldback current limiting. If the output fails by more than 50%, then the maximum sense voltage is progressively lowered to about one-fourth of its full value.

If the output exceeds 7.5% of the programmed value, then it is considered as an overvoltage (OV) condition. In such a case, the top MOSFET is immediately turned off and the bottom MOSFET is turned on indefinitely until the OV condition is removed. Current limiting is not active during an OV. If the output returns to a nominal level, then normal operation resumes. If the OV persists a long time, the current through the inductor could exceed its maximum rating.

OPTI-LOOP Compensation

OPTI-LOOP compensation, through the availability of the ITH pin, allows the transient response to be optimized for a wide range of loads and output capacitors. The ITH pin not only allows optimization of the control loop behavior but also provides a test point for the step-down regulator's DC-coupled and AC-filtered closed-loop response. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at this pin.

The ITH series R_{ITH} - C_{ITH1} filter sets the dominant pole-zero loop compensation. Additionally, a small capacitor placed from the ITH pin to SGND, C_{ITH2} , may be required to attenuate high frequency noise. The values can be modified to optimize transient response once the final PCB layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise

time of 1 μ s to 10 μ s will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The general goal of OPTI-LOOP compensation is to realize a fast but stable ITH response with minimal output droop due to the load step. For a detailed explanation of OPTI-LOOP compensation, refer to Application Note 76.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \cdot ESR$, where ESR is the effective series resistance of C_{OUT} . ΔI_{LOAD} also begins to charge or discharge C_{OUT} , generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

Connecting a resistive load in series with a power MOSFET, then placing the two directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load-step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated feedback loop response.

The gain of the loop increases with R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH1} . If R_{ITH} is increased by the same factor that C_{ITH1} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor, C_{FF} , can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R_{FB2} which improves the phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate overall performance of the step-down regulator.

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In some applications, a more severe transient can be caused by switching in loads with large ($>10\mu\text{F}$) input capacitors. If the switch connecting the load has low resistance and is driven quickly, then the discharged input capacitors are effectively put in parallel with C_{OUT} , causing a rapid drop in V_{OUT} . No regulator can deliver enough current to prevent this problem. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses:

1. I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through the inductor L, but is chopped between the top and bottom MOSFETs.
2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V.

3. INTV_{CC} current. This is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ , moves from INTV_{CC} to ground. The resulting dQ/dt is a current out of INTV_{CC} that is typically much larger than the controller I_Q current.

Supplying INTV_{CC} power through EXTV_{CC} could save several points of efficiency, especially for high V_{IN} applications. Connecting EXTV_{CC} to an output-derived source will scale the V_{IN} current required for the driver and controller circuits by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application, 10mA of INTV_{CC} current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in cabling, fuses or batteries.

Other losses, which include the C_{OUT} ESR loss, bottom MOSFET reverse-recovery loss and inductor core loss generally account for less than 2% additional loss.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current there is no change in efficiency.

Power losses in the switching regulator will reflect as a longer than ideal on-time. This efficiency accounted on-time in continuous mode can be calculated as:

$$t_{\text{ON(REAL)}} \approx \frac{t_{\text{ON(IDEAL)}}}{\text{Efficiency}}$$

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Design Example

Consider a step-down converter with $V_{IN} = 6V$ to $24V$, $V_{OUT} = 1.2V$, $I_{OUT(MAX)} = 15A$, and $f = 350kHz$ (see Figure 9).

The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}} \right)$$

Using a 20k resistor from V_{OSNS}^+ to V_{OSNS}^- , the top feedback resistor is also 20k.

The frequency is programmed by:

$$R_T [k\Omega] = \frac{41550}{f[kHz]} - 2.2 = \frac{41550}{350} - 2.2 \approx 116.5k$$

Select the nearest standard value of 115k.

The minimum on-time occurs for maximum V_{IN} and should be greater than 65ns, which is the best that the LTC3613 can achieve. The minimum on-time for this application is:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \cdot f} = \frac{1.2V}{24V \cdot 350kHz} \approx 143ns$$

Set the inductor value to give 40% ripple current at maximum V_{IN} :

$$L = \frac{1.2V}{350kHz \cdot 40\% \cdot 15A} \cdot \left(1 - \frac{1.2V}{24V} \right) \approx 0.54\mu H$$

Select 0.56μH, which is the nearest standard value.

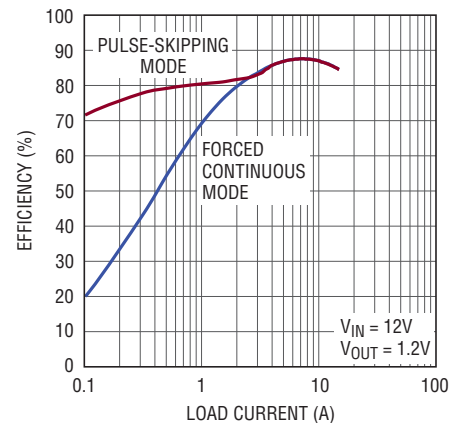
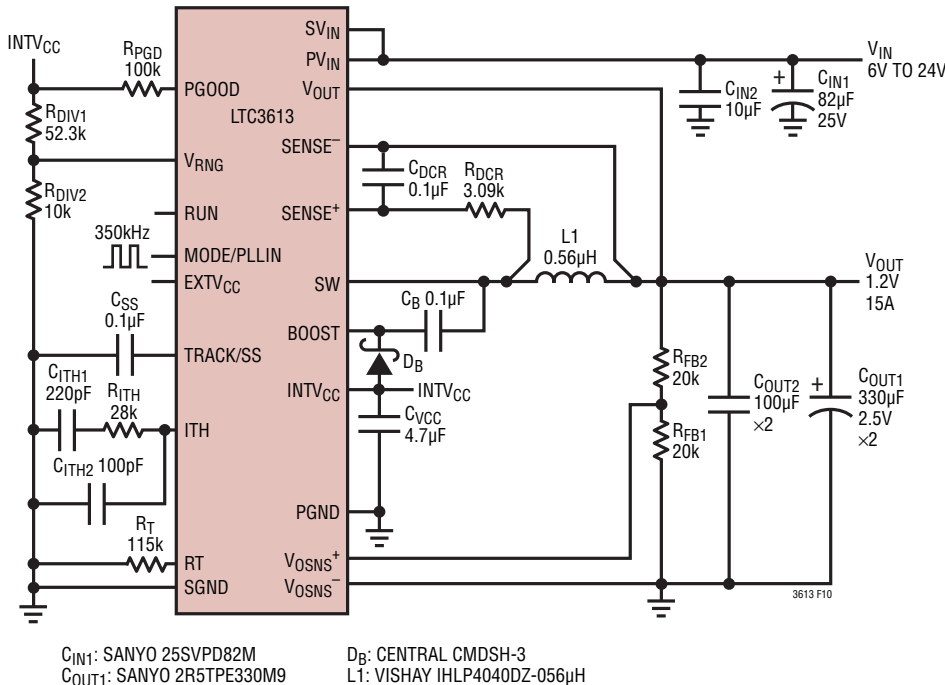


Figure 9. 1.2V, 15A, 350kHz Step-Down Converter

APPLICATIONS INFORMATION

The resulting maximum ripple current is:

$$\Delta I_L = \frac{1.2V}{350kHz \cdot 0.56\mu H} \cdot \left(1 - \frac{1.2V}{24V}\right) \approx 5.8A$$

Often in high power applications, DCR current sensing is preferred over R_{SENSE} in order to maximize efficiency. In order to determine the DCR filter values, first the inductor manufacturer has to be chosen. For this design, the Vishay IHLP-4040DZ-01 model is chosen with a value of $0.56\mu H$ and $DCR_{MAX} = 1.8m\Omega$. This implies that:

$$\begin{aligned} V_{SENSE(MAX)} &= DCR_{MAX} \text{ at } 25^\circ C \cdot [1 + 0.4\% (T_{L(MAX)} - 25^\circ C)] \cdot [I_{OUT(MAX)} - \Delta I_L/2] \\ &= 1.8m\Omega \cdot [1 + 0.4\% (100^\circ C - 25^\circ C)] \cdot [15A - 5.8A/2] \\ &\approx 28.3mV \end{aligned}$$

The maximum sense voltage is within the range that LTC3613 can handle without any additional scaling. Therefore, the DCR filter consists of a simple RC filter across the inductor. If the C is chosen to be $0.1\mu F$, then the R can be calculated as:

$$R_{DCR} = \frac{L}{DCR_{MAX} \cdot C_{DCR}} = \frac{0.56\mu H}{1.8m\Omega \cdot 0.1\mu F} \approx 3.11k$$

The closest standard value is 3.09k.

The resulting value of V_{RNG} with a 50% design margin factor is:

$$\begin{aligned} V_{RNG} &= V_{SENSE(MAX)}/0.05 \cdot MF \\ &= 28.3mV/0.05 \cdot 1.5 \approx 850mV \end{aligned}$$

To generate the V_{RNG} voltage, connect a resistive divider from $INTV_{CC}$ to SGND with $R_{DIV1} = 52.3k$ and $R_{DIV2} = 10k$.

Select C_{IN} to give an RMS current rating greater than 7A at $75^\circ C$. The output capacitor C_{OUT} is chosen for a low ESR of $4.5m\Omega$ to minimize output voltage changes due to inductor ripple current and load steps. The output voltage ripple is given as:

$$\begin{aligned} \Delta V_{OUT(RIPPLE)} &= \Delta I_{L(MAX)} \cdot ESR = (5.8A)(4.5m\Omega) \\ &\approx 26mV \end{aligned}$$

However, a 0A to 10A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD} \cdot ESR = (10A)(4.5m\Omega) = 45mV$$

Optional $100\mu F$ ceramic output capacitors are included to minimize the effect of ESR and ESL in the output ripple and to improve load step response.

PC Board Layout Checklist

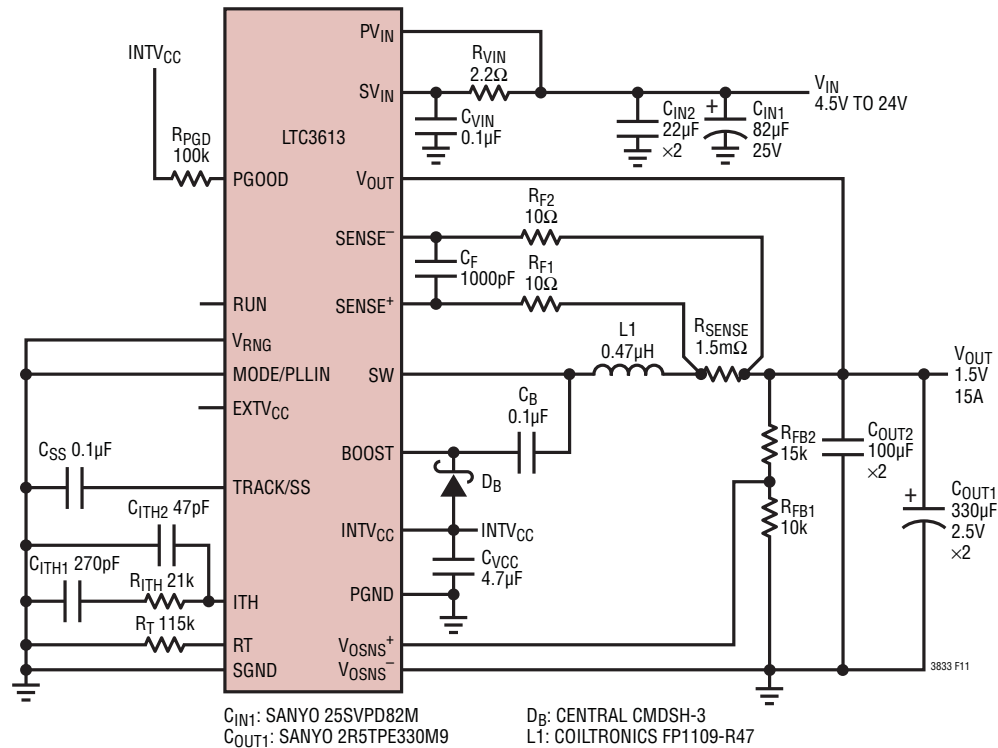
When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3613.

- Multilayer boards with dedicated ground layers are preferable for reduced noise and for heat sinking purposes. Use wide rails and/or entire planes for V_{IN} , V_{OUT} and PGND nodes for good filtering and minimal copper loss. Flood unused areas of all layers with copper for better heat sinking.
- Keep signal and power grounds separate except at the point where they are shorted together. Short signal and power ground together only at a single point with a narrow PCB trace (or single via in a multilayer board). All power train components should be referenced to power ground and all small-signal components (e.g., C_{ITH1} , R_T , C_{SS} etc.) should be referenced to signal ground.
- Place C_{IN} , inductor, sense resistor (if used), and primary C_{OUT} capacitors close together in one compact area. The SW node should be compact but be large enough to handle the inductor currents without large copper losses. Connect PV_{IN} as close as possible to the (+) plate of C_{IN} capacitor(s) that provides the bulk of the AC current (these are normally the ceramic capacitors), and connect PGND as close as possible to the (-) terminal of the same C_{IN} capacitor(s). The high dI/dt loop formed by C_{IN} , the top MOSFET, and the bottom MOSFET should have short leads and PCB trace lengths to minimize high frequency EMI and voltage stress from inductive ringing. The (-) terminal of the primary C_{OUT} capacitor(s) which filter the bulk of the inductor ripple current (these are normally the ceramic capacitors) should also be connected close to the (-) terminal of C_{IN} .

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- Place the BOOST, PV_{IN}, SW, and PGND pins facing the power train components. Keep high dV/dt signals on BOOST and SW away from sensitive small-signal traces and components.
- For R_{SENSE} current sensing, place the sense resistor close to the inductor on the output side. Use a Kelvin (4-wire) connection across the sense resistor and route the traces together as a differential pair. RC filter the differential sense signal close to SENSE⁺/SENSE⁻ pins, placing the filter capacitor as close as possible to the pins. For DCR sensing, Kelvin connect across the inductor and place the DCR sensing resistor closer to the SW node and further away from the SENSE⁺/SENSE⁻ pins. Place the DCR capacitor close to the SENSE⁺/SENSE⁻ pins.
- Place the resistive feedback divider R_{FB1/2} as close as possible to V_{OSNS}⁺/V_{OSNS}⁻ pins and route the remote output and ground traces together as a differential pair and terminate as close to the regulation point as possible (preferably Kelvin connect across the capacitor at the remote output point).
- Place the ceramic C_{VCC} capacitor as close as possible to the INTV_{CC} and PGND pins. Likewise, the C_B capacitor should be as close as possible to BOOST and SW pins. These capacitors provide the gate charging currents for the onboard power MOSFETs.
- Place small-signal components as close to their respective pins as possible. This minimizes the possibility of PCB noise coupling into these pins. Give priority to V_{OSNS}⁺/V_{OSNS}⁻, SENSE⁺/SENSE⁻, ITH, RT and V_{RNG} pins. Use sufficient isolation when routing a clock signal into MODE/PLLIN pin so that the clock does not couple into sensitive small-signal pins.
- Filter the SV_{IN} input to the LTC3613 with a simple RC filter close to the pin. The RC filter should be referenced to signal ground.

APPLICATIONS INFORMATION



Efficiency

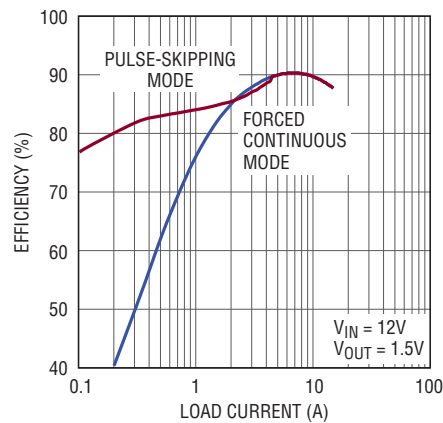


Figure 10. 1.5V, 15A, 350kHz High Current Step-Down Converter

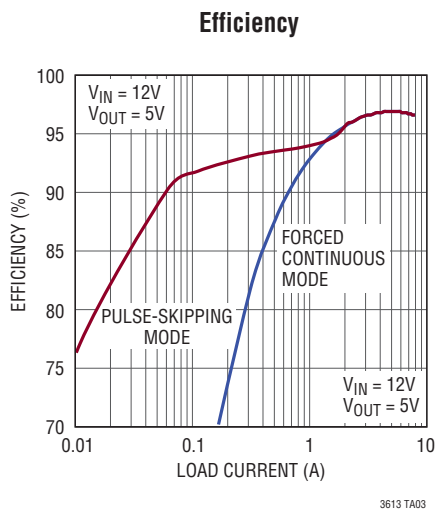
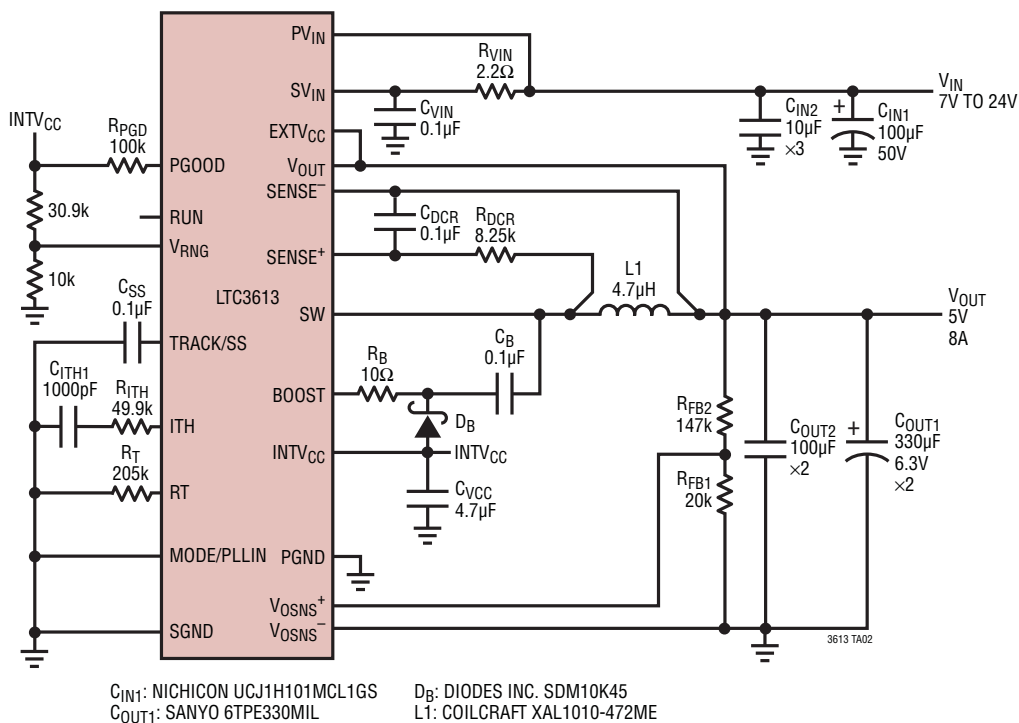
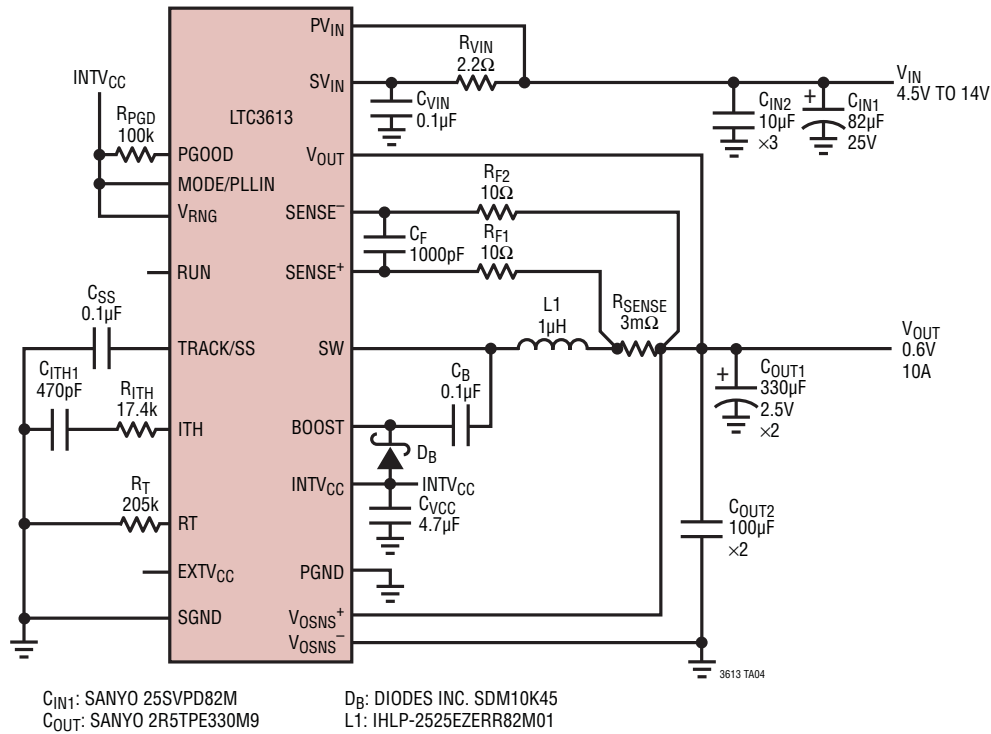


Figure 11. 5V, 8A, 200kHz High Efficiency Step-Down Converter

TYPICAL APPLICATIONS



Efficiency

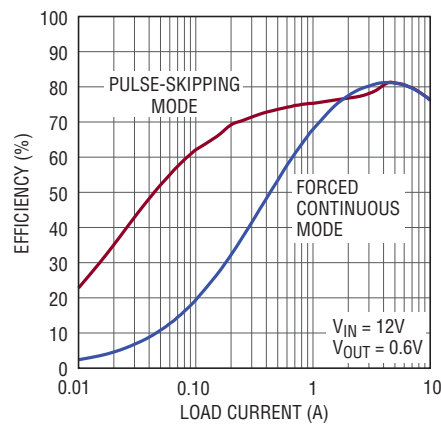


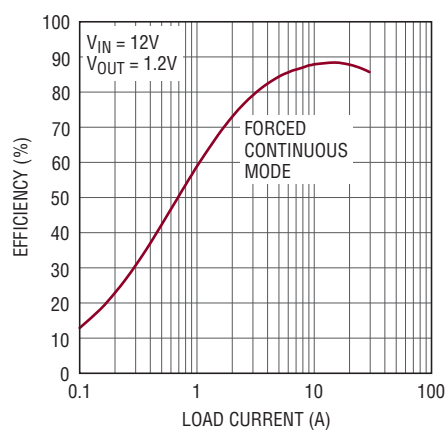
Figure 12. 0.6V, 10A, 200kHz Low Output Voltage Step-Down Converter



Figure 13. 2 Phase, 1.2V, 30A, 350kHz Step-Down Converter

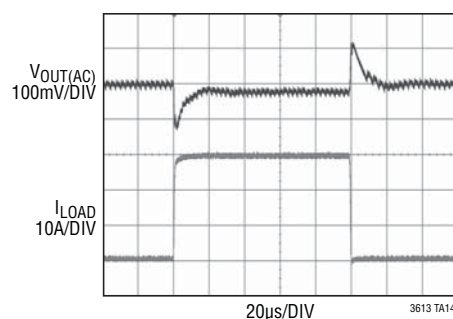
TYPICAL APPLICATIONS

Efficiency



3613 TA013

Transient Response



3613 TA14

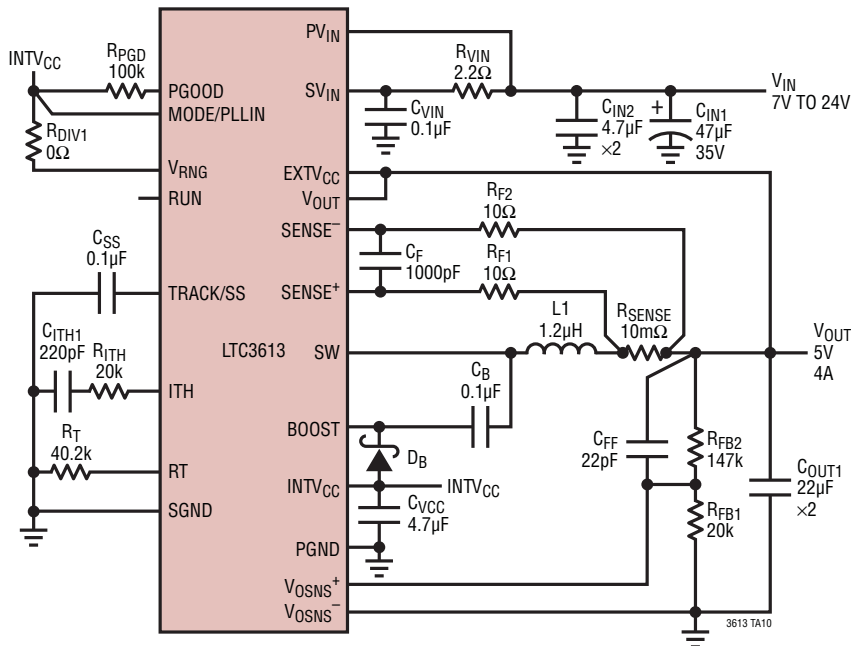
LOAD STEP = 0A TO 30A
 $V_{IN} = 12V$

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/12	Clarified Electrical Characteristics	3, 4
		Clarified PIn Functions	8
		Modified Application Circuit	33

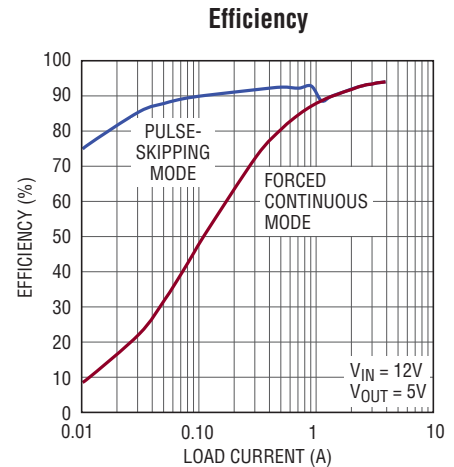
TYPICAL APPLICATION

High Frequency 5V, 4A, 1MHz Step-Down Converter



CIN1: KEMET T521X476M035ATE070
 DB: DIODES, INC. SDM10K45

L1: WÜRTH 744313120



3613 TA11

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3602	2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 4.5V to 10V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, TSSOP-16E Packages
LTC3608	18V, 8A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 4V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 7mm × 8mm QFN-52 Package
LTC3610	24V, 12A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 4V to 24V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 9mm × 9mm QFN-64 Package
LTC3611	32V, 10A (I_{OUT}), 1MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 4V to 32V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 900µA, I_{SD} < 15µA, 9mm × 9mm QFN-64 Package
LTC3414/ LTC3416	4A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, I_{SD} < 1µA, TSSOP20E Package
LTC3415	7A (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 450µA, I_{SD} < 1µA, 5mm × 7mm QFN-38 Package
LTC3418	8A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} : 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 380µA, I_{SD} < 1µA, 5mm × 7mm QFN-38 Package
LTM4600HV	10A Complete Switch Mode Power Supply	92% Efficiency, V_{IN} : 4.5V to 28V, V_{OUT} : 0.6V, True Current Mode Control, Ultrafast Transient Response
LTM4601HV	12A Complete Switch Mode Power Supply	92% Efficiency, V_{IN} : 4.5V to 28V, V_{OUT} : 0.6V, True Current Mode Control, Ultrafast Transient Response
LTM4602HV	6A Complete Switch Mode Power Supply	92% Efficiency, V_{IN} : 4.5V to 28V, V_{OUT} : 0.6V, True Current Mode Control, Ultrafast Transient Response
LTM4603HV	6A Complete Switch Mode Power Supply	93% Efficiency, V_{IN} : 4.5V to 28V, with PLL, Output Tracking and Margining

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